Amendment to the Claims:

The claims under examination in this application, including their current status and changes proposed in this paper, are respectfully presented.

1 (currently amended). A digital system comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases, wherein the microprocessor comprises:

program fetch circuitry operable to perform a first portion of the plurality of pipeline phases;

instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases; and

at least a first functional unit connected to receive control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases, wherein the first functional unit comprises:

byte intermingling circuitry connected to receive a ~~first~~ single source operand having an ordered plurality of fields ~~and a second source operand having an ordered plurality of fields~~ and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable, responsive to one of a plurality of byte intermingling instructions, to place ~~non-contiguous~~ data from a first selected field ~~fields~~ of the ~~first~~ single source operand ~~contiguously~~ in a lower field of a most significant portion of the destination operand, filling the remainder of the most significant portion of the destination operand with zeroes, and to place ~~non-contiguous~~ data from a second selected field ~~fields~~ of the ~~second~~ single source operand, the second selected field being contiguous with and less significant than the first selected field, ~~that are at the same positions as the selected fields from the first source operand, contiguously~~ in a lower field of a least significant portion of the destination operand, filling the remainder of the least significant portion of the destination operand with zeroes.

2 (currently amended). The digital system of Claim 1, wherein the byte intermingling circuitry is operable to receive the ~~first~~ single source operand ~~and second source operand~~ and to provide the destination operand during a single pipeline execution phase.

Claims 3 through 8 are canceled.

9 (currently amended). The digital system of Claim 1, further comprising a register file connected to the first functional unit for providing the ~~first and second~~ single source operand ~~operands~~ and connected to the first functional unit to receive the destination operand.

10 (original). The digital system of Claim 1, wherein each of the set of byte intermingling instructions has a field for identifying a predicate register.

11 (previously presented). The digital system of Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the microprocessor via a keyboard adapter;

a display, connected to the microprocessor via a display adapter;

radio frequency (RF) circuitry connected to the microprocessor; and

an aerial connected to the RF circuitry.

12 (currently amended). A method of operating a digital system having a microprocessor and a set of byte intermingling instructions, comprising the steps of:

fetching a byte intermingling instruction for execution;

fetching a ~~first~~ single source operand ~~and a second source operand~~ selected by the byte intermingling instruction, ~~each of~~ the single ~~first and second~~ source operand ~~operands~~ comprising an ordered plurality of fields; and

writing, ~~contiguously~~ into a lower field of a most significant portion of a destination operand, ~~non-contiguous~~ data from a first selected ~~ones of the plurality of fields from~~ field of the ~~first~~ single source operand and filling the remainder of the most significant portion of the destination operand with zeroes, and writing, ~~contiguously~~ into a lower field of a least significant portion of the destination operand, ~~non-contiguous~~ data from a second selected ~~ones of the plurality of fields from~~ field of the ~~second~~ single source operand, the second selected

field being contiguous with and less significant than the first selected field, ~~that are at the same positions as the selected fields of the first source operand~~ and filling the remainder of the least significant portion of the destination operand with zeroes, the data being selected in accordance with the byte intermingling instruction.

13 (canceled).

14 (previously presented). The method of Claim 12, wherein the step of writing is performed during a single execution phase of the microprocessor.

15 (currently amended). The method of Claim 12, wherein the ~~writing step contiguously writes most significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand and contiguously writes most significant bytes of a plurality of fields selected from~~ first selected field is a most significant byte of the ~~first~~ single source operand, and wherein the second selected field is a next most significant byte of the single source ~~into the most significant portion of the destination~~ operand.

16 (currently amended). The method of Claim 12, wherein the ~~writing step contiguously writes least significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand and contiguously writes least significant bytes of a plurality of fields selected from~~ second selected field is a least significant byte of the ~~first~~ single source operand, and wherein the first selected field is a second least significant byte of the single source ~~into the most significant portion of the destination~~ operand.

Claims 17 through 19 are canceled.